CLAIMS

What is claimed is:

1. A method for forming salicides with reduced junction leakage comprising the steps of:

providing a semiconductor process wafer comprising a silicon substrate;

controllably inducing amorphization within the silicon substrate to a form a first amorphous region having a first predetermined depth measured from the silicon substrate surface;

carrying out at least one first thermal annealing process to controllably partially recrystallize the first amorphous region to produce a second amorphous region having a second predetermined depth less than the first predetermined depth;

depositing a metal layer over selected areas of the silicon substrate comprising the second amorphous region; and,

carrying out at least one second thermal annealing process to form a metal silicide.

2. The method of claim 1, wherein the metal silicide is formed substantially above an interface comprising the second amorphous region and crystalline silicon.

3. The method of claim 1, wherein the silicon substrate comprises single crystalline silicon in one of (111) and (100) orientation.

4. The method of claim 1, wherein the step of inducing amorphization comprises at least one ion implantation process.

5. The method of claim 4, wherein the at least one ion implantation process comprises ions selected from the group consisting of B, P, As, Si, Ge, O, C, and N.

6. The method of claim 4, wherein the at least one ion implantation process comprises a source/drain implant.

7. The method of claim 4, wherein the at least one ion implantation process comprises implanting O, C, and N in an upper surface of the first amorphous region to control the recrystallization rate in the at least one first thermal annealing process.

8. The method of claim 1, wherein the first amorphous region is formed at a depth of from about 10 nm to about 500 nm.

9. The method of claim 1, wherein the second amorphous region is formed at a depth of from about 5 nm to about 60 nm.

10. The method of claim 1, wherein the metal is at least one of cobalt and titanium.

11. The method of claim 1, wherein the metal silicide is a self-aligned metal silicide.

12. The method of claim 1, further comprising wet etching unsilicided areas of the metal layer with a wet etching solution leave salicides covering exposed silicon and polysilicon areas.

13. The method of claim 12, wherein the exposed silicon and polysilicon areas comprise at least one of a gate electrode, a source region, and drain region.

14. The method of claim 13, wherein the exposed silicon and polysilicon areas comprise a CMOS transistor having a design rule of less than about 0.25 microns.

15. A method for forming cobalt salicides with reduced CoSi spiking in sub quarter-micron and nanometer micro-electronic circuits comprising the steps of:

providing a semiconductor process wafer comprising a MOSFET gate structure formed over a silicon substrate;

inducing amorphization within the silicon substrate to a form a first amorphous region having a first predetermined depth measured from the silicon substrate surface;

carrying out at least one first thermal annealing process to controllably partially recrystallize the first amorphous region to produce a second amorphous region having a second predetermined depth less than the first predetermined depth;

depositing a layer of cobalt metal over the semiconductor process wafer including the second amorphous region; and,

carrying out at least one second thermal annealing process to form a cobalt silicide ($CoSi_2$) wherein an interface comprising the second amorphous region and crystalline silicon inhibits Co diffusion to reduce Co spiking.

16. The method of claim 15, wherein the metal silicide is formed substantially above the interface.

17. The method of claim 15, wherein the at least one first thermal annealing process comprises a temperature from about 500 °C to about 650 °C.

18. The method of claim 15, wherein the step of inducing amorphization comprises at least one ion implantation process.

19. The method of claim 18, wherein the at least one ion implantation process comprises ions selected from the group consisting of B, P, As, Si, Ge, O, C, and N.

20. The method of claim 18, wherein the at least one ion implantation process comprises a source/drain implant.

21. The method of claim 15, wherein the second amorphous region is formed at a depth of from about 5 nm to about 60 nm.

22. The method of claim 15, further comprising wet etching unsilicided areas of the cobalt layer with a wet etching solution to leave cobalt salicided areas covering exposed silicon and polysilicon areas.

23. The method of claim 22, wherein the exposed silicon and polysilicon areas comprise at least one of a gate electrode, a source region, and drain region.

24. The method of claim 15, wherein the MOSFET device comprises a design rule of less than about 0.25 microns.

25. The method of claim 15, wherein the MOSFET device comprises a design rule of less than about 0.10 microns.